

IN THE SPECIFICATION:

Please replace the Abstract of the Disclosure with the following amended Abstract of the Disclosure:

To generate a signal when a target temperature is reached, a temperature detector circuit is provided with comprises a first and second current sources connected in series, of which the first current source generates a PTAT current and the second current source is supplied with a temperature-independent reference voltage to generate a second current proportional to the reference voltage. The first and second currents are a first and second reference currents, respectively, at a reference temperature, and the first and second current sources are configured such that the ratio of the second reference current to the first reference current is proportional to the ratio of the target temperature to the reference temperature.

Please replace the paragraph at Page 6, Line 10 – Page 7, Line 5 with the following amended paragraph:

Fig. 3 is a detailed circuit of an example for the temperature detector circuit 20 in Fig. 2. The temperature detector circuit 30 comprises a PTAT current generator having a resistor 34 connected with a pair of transistors 35 and 36. The transistor 35 is connected to the reference branch 50 of a current mirror, and the transistor 36 is connected to the mirror branch 52 of

the current mirror. Another mirror branch 54 of the current mirror outputs a current I_1 , and the mirror branch 54 is also connected to another current mirror 59, the gate of an output transistor 38 and an output capacitor 66. The drain of the NMOS transistor 38 is connected to another mirror branch 56 of the current mirror and an output buffer 42, and the latter has an output 40 to provide a signal when the target temperature T_T is reached. On the other hand, a transconductive amplifier composed of an operational amplifier 64 and an NMOS transistor 62 is connected to a resistor transistor 46. The non-inverse input 48 of the operational amplifier 64 is connected to a temperature-independent reference voltage VREF, and the inverse input is connected to the resistor 46 and the source of the NMOS transistor 62. The drain current of the NMOS transistor 62 derives an output current I_2 through two current mirrors 57 and 59.